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TRANSMITTAL FORM

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Application Number	09/997,019
Filing Date	November 28, 2001
First Named Inventor	Whitman et al.
Group Art Unit	2823
Examiner Name	B. Kebede
Attorney Docket Number	2269-4294.2US (98-1208.02/US)

ENCLOSURES *(check all that apply)*

- ☒ Postcard receipt acknowledgment (attached to the front of this transmittal)
- ☒ Duplicate copy of this transmittal sheet in the event that additional filing fees are required under 37 C.F.R. § 1.16
- ☐ Preliminary Amendment
- ☐ Response to Restriction Requirement/Election of Species Requirement dated
- ☐ Amendment in response to office action dated
- ☐ Amendment under 37 C.F.R. § 1.116 in response to final office action dated
- ☐ Additional claims fee - Check No. in the amount of $
- ☐ Letter to Chief Draftsman and copy of FIGS. with changes made in red
- ☐ Transmittal of Formal Drawings
- ☐ Formal Drawings (sheets)
- ☐ Information Disclosure Statement, PTO/SB/08A (08-00); ☐ copy of cited references
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Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Brick G. Power — Registration No. 38,581
Signature	Brick G. Power
Date	October 3, 2005

CERTIFICATE OF MAILING

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Whitman et al.

Serial No.: 09/997,019

Filed: November 28, 2001

For: SPIN COATING FOR MAXIMUM FILL CHARACTERISTIC YIELDING A PLANARIZED THIN FILM SURFACE

Confirmation No.: 6139

Examiner: B. Kebede

Group Art Unit: 2823

Attorney Docket No.: 2269-4294.2US

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APPEAL BRIEF

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Attn: Board of Patent Appeals and Interferences

Sirs:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

I. REAL PARTY IN INTEREST

U.S. Serial No. 09/997,019 (hereinafter "the '019 Application), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc. The assignment was recorded with the United States Patent & Trademark Office (hereinafter the "Office") on at April 4, 2000, Reel 010729, Frame 0057. Accordingly, Micron Technology, Inc. is the real party in interest to the above-referenced appeal.

II. RELATED APPEALS AND INTERFERENCES

The final rejections in U.S. Application Serial No. 09/542,783 (hereinafter "the '783 Application"), the parent of the '019 Application, are subject to an appeal before the Board of Patent Appeals and Inteferences. An Appeal Brief was filed in the '783 Application on September 29, 2005.

The final rejections in U.S. Application Serial No. 09/944,230, a divisional of the '783 Application, are currently on appeal before the Board of Patent Appeals and Interferences (hereinafter "the Board"). A communication dated August 24, 2005, indicates that the file for that application has been forwarded to the Board.

The undersigned attorney is not aware of any other action, including any other appeals or interferences, currently ongoing before Board that may affect or be affected by the Board's decision in the appeal of the status of the '019 Application.

III. STATUS OF THE CLAIMS

Claims 1-22 are currently pending and under consideration in the above-referenced application.

Each of claims 1-22 stands rejected.

The rejections of claims 1-22 are being appealed.

IV. STATUS OF AMENDMENTS

The '019 Application was filed on November 28, 2001, as a divisional of the '783 Application. The '019 Application was originally filed with twenty-two (22) claims.

A Preliminary Amendment was mailed on February 12, 2002, to correct grammatical and formal errors in the claims.

A first Office Action on the merits was mailed by the Office on February 20, 2003. Each of claims 1-22 was rejected.

A response to the first Office Action was filed on May 23, 2003. That response included explanations of the patentability of claims 1-22.

As evidenced by a second, non-final Office Action dated August 29, 2003, the Examiner was convinced by Appellants' arguments and presented new grounds for rejecting claims 1-22

Thereafter, on December 1, 2003, an Amendment was filed. The Amendment of December 1, 2003, included minor claim revisions, in which some occurrences of the term "said" were removed and the remaining occurrences of the term "said" were replaced with the equivalent term "the." In addition, the Amendment included an analysis of the art that had been relied upon in rejecting claims 1-22, highlighting the patentability of the claims over the art.

A Final Office Action followed on February 19, 2004. In the Final Office Action, the rejections of claims 1-22 were maintained.

In an Amendment Under 37 C.F.R. § 1.116, which was filed on April 23, 2004, independent claim 1 was amended to remove the term "substantially," thus narrowing the number of issues that remained for purposes of this Appeal. In addition, further remarks were presented to establish the patentability of claims 1-22 over the art upon which the rejections of these claims were based.

In an Advisory Action dated May 10, 2004, the Office indicated that the Examiner was not convinced by the explanations that had been provided by Appellants, but that the proposed claim amendment would be entered upon appeal of the Examiner's rejections in the '019 Application.

A Notice of Appeal was promptly filed on May 19, 2004. Thereafter, on August 19, 2004, an Appeal Brief was filed with a petition and the appropriate fee for a one-month extension of time. An Examiner's Answer was mailed on October 19, 2004.

Following receipt of the Examiner's Answer, the '019 Application was withdrawn from Appeal for consideration of art that had been cited in a related application. Accordingly, a Request for Continued Examination (RCE) and Information Disclosure Statement were filed on November 5, 2004.

After the RCE was filed, the Examiner maintained her prior rejections of claims 1-22 in a non-final action dated December 1, 2004, a Final Office Action dated May 12, 2005, and an Advisory Action dated July 26, 2005. Additional explanations as to the patentability of claims 1-22 were provided in responses that were mailed on March 1, 2005, and July 12, 2005.

After these unsuccessful attempts to convince the Examiner of the impropriety of her rejections and of the patentability of claims 1-17, another Notice of Appeal was filed on August 1, 2005.

This Appeal Brief follows the Notice of Appeal and, as October 1, 2005, fell on a Saturday and this Appeal Brief is being submitted on Monday October 3, 2005, should be deemed to have been filed within two months of the filing date of the Notice of Appeal. 37 C.F.R. § 1.7.

V. SUMMARY OF THE INVENTION

The claims that have been considered in the '019 Application are drawn to methods for preparing the surface of semiconductor device structures for planarization.

In the inventive methods, a semiconductor device structure is provided. *See, e.g.,* Paragraphs **[0012]**, **[0045]**, **[0046]**, **[0052]**, **[0053]**, Figs. 7 and 12. The semiconductor device structure includes at least one recess in a surface thereof. *Id.* A first material layer substantially fills the recess and covers the surface. *Id.* A second material is then applied to the first material layer. *Id.* The second material is spread over the first material layer. *Id.* The resulting second material layer has a planar surface and does not require further planarization. *Id.*

VI. ISSUES

(A) Whether, under 35 U.S.C. § 102(e), claims 1, 2, 6, 7, and 10-22 recite subject matter which is novel over the subject matter described in U.S. Patent 6,461,932 to Wang (hereinafter "Wang");

(B) Whether, under 35 U.S.C. § 103(a), claims 3-5 are allowable for being drawn to subject matter which is patentable over the teachings of Wang, in view of teachings from U.S. Patent 6,117,486 to Yoshihara (hereinafter "Yoshihara"); and

(C) Whether claims 8 and 9 recite subject matter which, under 35 U.S.C. § 103(a), is patentable over teachings from Wang and U.S. Patent 6,228,711 to Hsieh (hereinafter "Hsieh").

VII. ARGUMENT

A. REJECTIONS UNDER 35 U.S.C. § 102(e)

Claims 1, 2, 6, 7, and 10-22 stand rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by the subject matter disclosed in Wang.

1. RELEVANT LAW

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The plain language of a reference constitutes its express description. M.P.E.P. § 2125 provides that "[d]rawings and pictures can anticipate claims is they clearly show the structure which is claimed," but cautions that the "drawings must be evaluated for what they reasonably disclose and suggest to one of ordinary skill in the art." This rule is based, at least in part, upon the holding in *In re Aslanian,* 200 USPQ 500 (C.C.P.A. 1979), in which the court directed "[w]e

evaluate and apply the teachings of all relevant references on the basis of what they reasonably disclose and suggest to one skilled in the art . . ." In *Aslanian,* the court was evaluating the relevance of drawings of a design patent as prior art to the claims of a patent application. Relative dimensions were not at issue, indicating that the guidance provided by M.P.E.P. § 2125 merely discusses relative dimensions of features of an illustrated object as an example of something that may not be reasonably disclosed or suggested to one of ordinary skill in the art.

M.P.E.P. § 2125 also indicates that arguments about illustrated drawing features, such as proportions and dimensions (*e.g.,* planarity or nonplanarity), are of little value when the specification does not specify that the drawings may be relied upon for such a purpose. Neither the M.P.E.P. nor the relevant case law indicates, as the Examiner has asserted, that an omission means that the subject matter illustrated in drawings must be taken at face value.

While dimensions are provided as an example of illustrated drawing featuers, nothing in the law requires that there be a "measured quantitative dimensional limitation" (Final Office Action, page 12) to avoid a rejection based on subject matter illustrated in the drawings of a reference.

2. REFERENCE RELIED UPON

Wang

Wang describes a process for creating a trench-isolated semiconductor structure "using a pre-smoothing technique to avoid difficulties such as dishing and premature silicon-nitride removal that might otherwise occur during chemical-mechanical polishing..." (hereinafter "CMP"). Col. 4, lines 48-51. While the avoidance of dishing and premature silicon nitride

removal may prevent some of the nonplanarities that might occur during CMP, dishing is only one type of nonplanarity; other types of nonplanarities may remain.

The process of Wang includes providing a dielectric layer 56 over a semiconductor surface, and covering the dielectric layer 56 with a "smoothening layer" 60. Col. 6, lines 23-28. The smoothening layer 60 has an upper smoothening surface 62 which is smoother than the upper dielectric surface 58 of the dielectric layer 56. Col. 6, lines 29-31. The smoothening layer 60 is applied either by a "deposition/spinning procedure" (col. 6, line 52, to col.7, line 14), a "deposition/flow" procedure (col. 7, lines 15-27), or a combination of these procedures (col. 7, lines 28-41). As a result of these processes, the upper smoothening surface 62 includes "slight depressions . . . at locations of the deepest parts of the depressed portion of upper dielectric surface 58." Col. 6, lines 32-37.

Once the smoothening layer 60 has been formed, the smoothening layer 60 and the dielectric layer 56 are removed by CMP until a portion of the underlying semiconductor device is exposed. Col. 7, line 42, to col. 8, line 25.

3. ANALYSIS

Fig. 4d of Wang illustrates the upper smoothening surface 62 of the smoothening layer 60 as being planar. The specification of Wang, however, does not disclose that the drawings may be relied upon at face value. Again, M.P.E.P. § 2125 indicates that the features that are illustrated in drawings, such as proportions and dimensions (*e.g.*, planarity or nonplanarity), are of little value when the specification does not state that the drawings may be relied upon for such a

purpose. Thus, according to M.P.E.P. § 2125, the drawings of Wang, specifically Fig. 4d, cannot be relied upon as disclosing that the upper smoothening surface 62 is substantially planar.

Moreover, when Fig. 4d is viewed in connection with the description of Wang, it is clear that Fig. 4d cannot be relied upon as showing a smoothening layer 60 with a planar upper smoothening surface 62. Instead, the description of Wang is limited to an upper smoothening surface 62 that is merely "largely planar." Wang even goes so far as to note that the term "largely planar" is a relative term and, thus, is merely used for the purpose of comparing the planarity of the upper smoothening surface 62 to the underlying and highly nonplanar upper dielectric surface 58. Col. 6, lines 35-36. Further, Wang explains that "slight depressions [are present] in upper smoothening surface 62 at locations of the deepest parts of the depressed portion of upper dielectric surface 58." Col. 6, lines 32-37.

a. Claim 1

Independent claim 1 is directed to a method for preparing a surface of a semiconductor device structure for planarization. The method of independent claim 1 includes, among other things, spreading a second material over a first material layer having a nonplanar surface so as to form a second material layer having a planar surface.

Wang lacks any express or inherent description of spreading a second material layer over a first material layer so as to form a second material layer having a planar surface, as recited in independent claim 1. Contrary to the assertion that has been made at page 11 of the Final Office Action, a "largely planar" surface 62 that may include "slight depressions" is not planar. Col. 6, lines 32-34.

Wang's description of the upper smoothening surface 62 as being "largely planar," as opposed to "planar," acknowledges that fact that conventional spin-on processes are incapable of forming material layers with planar surfaces. As the "Background" section of the specification of the '019 Application, at page 3, line 15, to page 4, line 29, points out, one of ordinary skill in the art would appreciate that the limitations of previously known spin-on methods, as well as material properties (*e.g.,* viscosity, solids content, surface tension, adherence to adjacent materials, etc.), may prevent a layer of material from having a substantially planar upper surface. *See, e.g.,* Van Zandt, P., Microchip Fabrication – Chapter 8, Photolithography—Preparation to Exposure, pages 176-178 and 185-187 (hereinafter "Van Zandt"). Further, Van Zandt, at page 185, evidently recognizing that a spun-on layer of photoresist will include valleys that are located over recesses in a semiconductor substrate, describes spun-on photoresist in terms of *layer* thickness (*e.g.,* 0.5 μm to 1.5 μm thick, with variations of ± 0.01 μm) rather than in terms of surface planarity. U.S. Patent 6,117,486 to Yoshihara (hereinafter "Yoshihara") provides further evidence that the surfaces of spun-on photoresist layers may not be planar. Yoshihara, col. 1, line 18, to col. 2, line 17). Copies of both Van Zandt and Yoshihara are enclosed for the sake of convenience.

Therefore, Wang does not anticipate "spreading [a] second material over [a] first material layer so as to form a second material layer having a planar surface," as would be required to uphold the 35 U.S.C. § 102(e) rejection of independent claim 1.

It is also respectfully submitted that claims 2, 6, 7, and 10-22 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

b. Claim 10

In discussing the patentability of claim 10, which depends from claims 2 and 1, the Examiner has improperly focused on the examples described in the specification of the '019 Application rather than on the subject matter recited in claim 10. *See* Final Office Action, pages 14 and 15. In the method of claim 10, a stress buffer material is spread in such a way that at least one valley of a first material layer be at least partially filled with the stress buffer material while at least one peak of the first material layer remains substantially uncovered by the stress buffer material. The corresponding description of Wang, in contrast, is clearly limited to applying the smoothening layer 60 in such a manner that "the depressed portion[s] of upper dielectric surface 58 above trench[es] 54" are completely filled (col. 6, lines 26-27; Fig. 4d), while the peaks of the dielectric layer 56 are covered. None of the peaks of the dielectric layer 56 of Wang is exposed until after the CMP process has begun. *See* col. 7, line 65, to col. 8, line 4.

It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), the subject matter to which claim 10 is directed is allowable over the subject matter described in Wang.

c. Claim 13

Claim 13, which depends from claims 12, 11, 10, 2, and 1, is additionally allowable since Wang includes no express or inherent description that the dielectric layer 56 of the structure disclosed therein may be *etched* with selectivity over the smoothening layer 60 of the disclosed structure until a surface of at least one region of the dielectric layer 56 is in substantially the same plane as a surface of the smoothening layer 60.

The Examiner's persistence in maintaining the 35 U.S.C. § 102(e) rejection of claim 13 demonstrates a misunderstanding of the differences between etching, as recited in claim 13, and the CMP process disclosed in Wang, which differences are and would have been readily apparent to those of ordinary skill in the art. Specifically, etching is a process by which a chemical etchant removes a material on its own. *See, e.g.,* Wolf, "Silicon Processing for the VLSI Era, Volume 1: Process Technology," pages 520-29 (Lattice Press, 1986); Van Zandt, at pages 221-33. Copies of portions of both of these references are enclosed for the sake of convenience. CMP, in contrast, is a process by which a material to be removed is oxidized by a slurry, and must be subsequently mechanically removed by way of a polishing pad. *See, e.g.,* "Chemical-mechanical planarization," http:/en.wikipedia.org/wiki/Chemical_mechanical_polish" (June 24, 2005); Wolf, "Silicon Processing for the VLSI Era, Volume 2: Process Integration," pages 238-39 (Lattice Press, 1990). Copies of portions of both of these references are enclosed for the sake of convenience.

It is through removal of the smoothening layer 60 by CMP, not etching, that surfaces of the smoothening layer 60 and the dielectric layer 56 are made substantially coplanar. *See* col. 7, line 65, to col. 8, line 4; Fig. 4e.

Accordingly, it is respectfully submitted that the subject matter recited in claim 13 is not anticipated under 35 U.S.C. § 102(e) by the subject matter described in Wang and, thus, is allowable over the subject matter described in Wang.

d. Claim 15

Claim 15, which depends from claims 13, 12, 11, 10, and 2, is additionally allowable since Wang includes no express or inherent description that the dielectric layer 56 and the smoothening layer 60 may be etched at substantially the same rate so as to expose a surface of the mask layer 44 adjacent a surface of a portion of the dielectric layer 56 in at least one recess, with the surfaces of the mask layer 44 and the dielectric layer 56 being located in substantially the same plane following such planarization. Rather than describing etching processes to remove both the smoothening layer 60 and the dielectric layer 56, the description of Wang is limited to use of CMP.

It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(e), claim 15 is drawn to subject matter which is allowable over the subject matter described in Wang.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(e) rejections of claims 1, 2, 6, 7, and 10-22 be reversed.

B. REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 3-5, 8, and 9 stand rejected under 35 U.S.C. § 103(a).

1. RELEVANT LAW

The standard for establishing and upholding a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. WANG IN VIEW OF YOSHIHARA

Claims 3-5 have been rejected under 35 U.S.C. § 103(a) for being directed to subject matter which is allegedly unpatentable over the subject matter taught in Wang, in view of teachings from Yoshihara.

a. ADDITIONAL REFERENCE RELIED UPON

Yoshihara

Yoshihara teaches a method for forming photoresist layers that have a "predetermined" "uniform thickness" without any "ripples" therein. *See, e.g.,* Col. 2, line 33; col. 11, lines 48-54, 62; Fig. 9. The phrase "uniform thickness" should not be confused with a "substantially planar" upper surface.

b. ANALYSIS

Claims 3-5 are each allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Moreover, it is respectfully submitted that the Office has not established a *prima facie* case of obviousness against any of claims 3-5, as would be required to uphold the 35 U.S.C. § 103(a) rejections of these claims.

It is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Wang with those of Yoshihara. Since Yoshihara teaches a process for forming a layer of uniform thickness, if the process taught in Yoshihara were used to form the smoothening layer 60 of Wang, the smoothening layer 60 would have a uniform thickness. It is clearly not possible for a layer which is formed over a nonplanar surface and which has a uniform thickness to have a planar surface. As a result, the smoothening surface 62 of the smoothening layer 60 would be every bit as nonplanar as the upper surface of the underlying dielectric layer 56. *See* Wang, Fig. 4d.

Since the only result of the asserted combination of teachings one of ordinary skill in the art could reasonably expect would differ from the subject matter recited in independent claim 1, from which claims 3-5 depend, it appears that any motivation to combine the teachings of Yoshihara and Wang in the asserted manner could only have been improperly gleaned by the Examiner from the subject matter described and claimed in the '019 Application.

It is also respectfully submitted that a person of ordinary skill in the art at the time of the invention would have no reason to expect that combining the teachings of Wang and Yoshihara in the manner that has been asserted would have been successful. Again, use of the spin-on process taught in Yoshihara to form the smoothening layer 60 of Wang would have merely resulted in a structure with a smoothening layer 60 of uniform thickness. Due to the uniform thickness of the resulting smoothening layer 60, the upper smoothening surface 62 thereof would

take on the same topography as the uneven upper surface of the underlying dielectric layer 56. Thus, one of ordinary skill in the art would have no reason to expect the asserted combination of teachings from Wang and Yoshihara to result in a smoothening layer 60 that has a planar upper smoothening surface 62, as would be required to render the subject matter recited in independent claim 1, from which claims 3-5 depend, obvious and, thus, unpatentable.

For these reasons, it is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 3-5 and, thus, that under 35 U.S.C. § 103(a) each of claims 3-5 is drawn to subject matter which is allowable over the teachings of Wang and Yoshihara, taken either individually or together.

3. WANG IN VIEW OF HSIEH

Claims 8 and 9 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over the teachings of Wang, in view of teachings from Hsieh.

Claims 8 and 9 are both allowable, among other reasons, for respectively depending directly and indirectly from claim 1, which is allowable.

In view of the foregoing, reversal of the 35 U.S.C. § 103(a) rejections of claims 3-5, 8, and 9 is respectfully requested.

VIII. CLAIMS APPENDIX

The current status of each claim that has been introduced into the '783 Application is set forth in CLAIMS APPENDIX to this Appeal Brief.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

XI. CONCLUSION

It is respectfully submitted that:

(A) Claims 1, 2, 6, 7, and 10-22 recite subject matter which, under 35 U.S.C. § 102(e), is novel over the subject matter described in Wang;

(B) Claims 3-5 are allowable under 35 U.S.C. § 103(a) for being drawn to subject matter which is patentable over the teachings of Wang, in view of teachings from Yoshihara; and

(C) Claims 8 and 9 recite subject matter which, under 35 U.S.C. § 103(a), is patentable over teachings from Wang and Hsieh.

In view of the foregoing, it is respectfully requested that the Examiner's rejections of claims 1-22 be reversed and that each of these claims be allowed.

Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously presented) A method for preparing a surface of a semiconductor device structure for planarization, comprising:

providing a semiconductor device structure including at least one recess formed in a surface thereof and a first material layer substantially filling the at least one recess and covering the surface, the first material layer having a nonplanar surface;

applying a second material to the first material layer; and

spreading the second material over the first material layer so as to form a second material layer having a planar surface without requiring subsequent planarization of the second material.

2. (Previously presented) The method of claim 1, wherein applying the second material comprises applying a stress buffer material to the first material layer.

3. (Previously presented) The method of claim 1, wherein the spreading comprises:

spinning the semiconductor device structure at a first speed;

gradually decreasing a rate of the spinning to a second speed; and

gradually increasing a rate of the spinning to a third speed.

4. (Previously presented) The method of claim 3, wherein spinning the semiconductor device structure at the second speed comprises permitting the second material within the at least one recess to at least partially set.

5. (Previously presented) The method of claim 3, wherein spinning the semiconductor device structure at the third speed comprises forming the second material over the surface to a desired thickness.

6. (Previously presented) The method of claim 1, wherein providing comprises providing a shallow trench isolation structure with the at least one recess comprising at least one trench formed in a surface of the shallow trench isolation structure.

7. (Previously presented) The method of claim 6, wherein providing further comprises providing the shallow trench isolation structure with the first material layer comprising an electrical insulator material.

8. (Previously presented) The method of claim 1, wherein providing comprises providing a semiconductor device structure with the at least one recess comprising at least one dual damascene trench formed therein.

9. (Previously presented) The method of claim 8, wherein providing further comprises providing a semiconductor device structure with the first material layer comprising conductive material.

10. (Previously presented) The method of claim 2, wherein spreading comprises at least partially filling at least one valley of the first material layer with the stress buffer material

while leaving at least one peak of the first material layer substantially uncovered by the stress buffer material.

11. (Previously presented) The method of claim 10, further comprising planarizing at least the first material layer.

12. (Previously presented) The method of claim 11, wherein planarizing comprises etching at least one region of the first material layer exposed through the stress buffer material with selectivity over the stress buffer material.

13. (Previously presented) The method of claim 12, wherein etching is effected until a surface of the at least one region is in substantially the same plane as a surface of the stress buffer material.

14. (Previously presented) The method of claim 13, wherein planarizing further comprises abrasively planarizing the stress buffer material and the at least one region to expose the surface of the semiconductor device structure adjacent the at least one recess, the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following planarizing.

15. (Previously presented) The method of claim 13, wherein planarizing further comprises concurrently etching the first material layer and the stress buffer material at

substantially the same rate so as to expose the surface of the semiconductor device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following the planarizing.

16. (Previously presented) The method of claim 11, wherein planarizing is effected until the surface of the semiconductor device structure is exposed through the first material layer.

17. (Previously presented) The method of claim 16, wherein etching is effected until a surface of the first material layer in the at least one recess is in substantially the same plane as the surface of the semiconductor device structure.

18. (Previously presented) The method of claim 16, further comprising removing the stress buffer material from the semiconductor device structure.

19. (Previously presented) The method of claim 2, wherein spreading comprises forming a substantially planar surface over the semiconductor device structure.

20. (Previously presented) The method of claim 19, further comprising planarizing at least the first material layer.

21. (Previously presented) The method of claim 20, wherein planarizing comprises substantially concurrently abrasively planarizing the stress buffer material and the first material layer to expose the surface of the semiconductor device structure adjacent the at least one recess, the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following planarizing.

22. (Previously presented) The method of claim 20, wherein planarizing comprises substantially concurrently etching the first material layer and the stress buffer material at substantially the same rate so as to expose the surface of the semiconductor device structure adjacent the at least one recess with the surface of the semiconductor device structure and a surface of the first material layer in the at least one recess being located in substantially the same plane following planarizing.

Microchip Fabrication

A Practical Guide to Semiconductor Processing

Peter Van Zant

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Parameter	Negative	Positive
Aspect Ratio (Resolution)		Higher
Adhesion	Better	
Exposure Speed	Faster	
Pinhole Count		Lower
Step Coverage		Better
Cost		Higher
Developers	Organic Solvents	Aqueous
Strippers		
Oxide Steps	Acid	Acid
Metal Steps	Chlorinated Solvent Compounds	Simple Solvents

Figure 8.20 Comparison of negative and positive resists.

these lines use negative resists. Figure 8.20 shows a comparison of properties of the two resists.

Physical Properties of Photoresists

The performance factors just detailed are related to a number of physical and chemical properties of the resist. The properties are discussed in the following text. The influence of a particular property on the process is discussed in the process sections.

Solids content

A photoresist is a liquid that is applied to the wafer by a spinning technique. The thickness of resist left on the wafer is a function of the spin step parameters and several resist properties (two of which are the solids content and viscosity).

Recall that the photoresist is a suspension of polymers, sensitizers and additives in a solvent. Different resists will contain different amounts of these solids. The amount is referred to as the solids content of the resist and is expressed as the weight percent in the resist. Solids content is measured by evaporating off the solvent and weighing the amount of solids left. Solids contents are in the 20 to 40 per cent range.[4]

Viscosity

Viscosity is the quantitative measure of liquid flow. High-viscosity liquids, such as tractor oils, flow in a sluggish manner. Low-viscosity liquids, such as water, flow more readily. In both cases, the mechanism of flow is the same. The molecules in the liquid roll over each other as the liquid is being poured. As the molecules roll about, they

exists an attraction between them that acts as an internal friction. Viscosity is the measurement of that friction.

Viscosity is measured by several techniques. One is the falling ball viscosimeter. In this instrument, a ball of measured size and weight is dropped into a tube of the liquid and timed as it passes between two marks. The higher the viscosity of the liquid, the longer it takes the ball to transist the marked distance. Another technique is the Ostwalk-Cannon-Fenske method, which is a timed measurement for a given amount of a liquid to pass through a given orifice.

Most photoresist manufacturers measure viscosity with a rotating vane in the resist. The higher the viscosity, the more force is required to move the vane through the liquid at a constant speed. The rotating-vane apparatus illustrates the force-related character of viscosity.

The unit of viscosity is the centipoise. It is named after the French scientist Poisseulle who investigated the viscous flow of liquids. The poise is equal to one dyne second per centimeter. Photoresist is measured in centipoise. One centipoise is one-hundredth of a poise. The viscosity unit of centipoise is more correctly named the *absolute viscosity*.

Another viscosity unit used by photoresist manufacturers is centistokes. This value is calculated from the absolute viscosity (centipoise) divided by the density of the resist. This value is called the *kinematic viscosity*. Viscosity varies with temperature; therefore, its specified value is stated at a particular temperature, usually 25°C. Viscosity is a major parameter determining the resist thickness during the spin process. Viscosity is closely related to the solids content. The higher the solids content, the higher the viscosity.

Surface tension

The surface tension of a resist also influences the outcome at spin. Surface tension is a measure of the attractive forces in the surface of the liquid (Fig. 8.21). Liquids with high surface tension flow less readily on a flat surface. It is the surface tension that draws a liquid into a spherical shape on a surface or in a tube.

Index of refraction

When the resist-covered wafer surface is being exposed, the transparent resist is part of an optical system. As such, its optical properties must be specified and controlled. One property of transparent films sitting on reflective substrates (resist on a wafer) is that a light ray impinging on the surface at an angle will be bent as it passes through

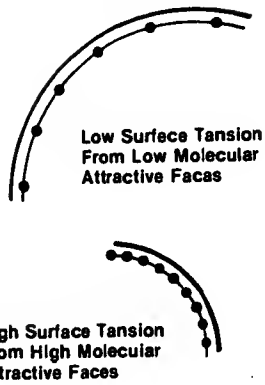

Figure 8.21 Surface tension.

the film. This comes about as the light ray is slowed up in the material. The index of refraction is a measurement of the speed of light in a material compared to its speed in air, as shown in Fig. 8.22. It is calculated as the ratio of the reflecting angle to the impinging angle. For photoresists, the index of refraction is close to that of glass, approximately 1.45.

Storage and Control of Photoresists

Photoresists are delicate high-technology mixtures. Great care and precision go into their manufacture. Once a photomasking process is developed, its continuing success depends on the day-in, day-out control of the process parameters and a consistent photoresist product

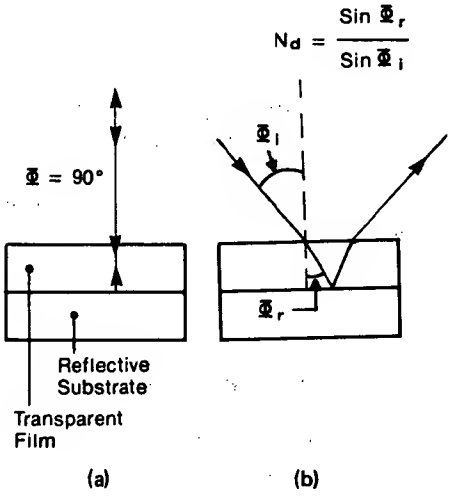

Figure 8.22 Index of refraction. (*a*) 90° incident light; (*b*) angled light is refracted in the transparent film.

heated to the vapor point and the wafers are suspende
for coating.

A newer technique is vacuum vapor priming, which use
flask of HMDS connected to a vacuum oven or single-wafer
The wafers are first heated in the oven in a nitrogen atmosp
ter a temperature of about 150°C is reached, the atmos
switched to a vacuum. Once the vacuum level is reached, a
opened and HMDS vapors are drawn into the chamber by
pressure. Within the chamber, the wafers become completel
as the vapors fill the entire chamber. This method has shown
hesion longevity even in the presence of high humidity.[6]

Vacuum vapor priming offers the additional advantage o
bined dehydration bake and prime step and a significant red
HMDS usage. In a production area that typically uses g
HMDS per week, switching to vacuum vapor priming will re
age to pints per month. Vacuum vapor priming practiced in
type oven adds an additional step to the process. Many a
spinner systems offer in-line vapor primers.

Photoresist spinning

The purpose of the photoresist application step is the establis
a thin, uniform, defect-free film of photoresist on the wafer
These qualities are easy to state, but they require sophisticate
ment and stringent controls to achieve. A typical resist laye
from 0.5 to 1.5 μm in thickness and has to have a uniformity c
minus only 0.01 μm (100 Å). This variation is 1 percent of a
thickness.

The usual methods of applying thin layers of liquids to surf
brushing, rolling, and dipping. None of these methods is ade
achieve the quality resist film necessary for photomaski
method used is spinning, which was briefly described in the se
priming. Spinners are built in manual, semiautomatic, and a
designs. The systems differ in the degree of automation and
scribed in the following text. However, the deposit of the film
wafer is common to each of the systems.

The static spin process. The wafer that is ready for spinnir
priming) is on the vacuum chuck. Several cubic centimeters
the photoresist is deposited in the center of the wafer (Fig. 8
allowed to spread out into a puddle. The puddle is allowed t
until it covers the majority of the wafer surface. The size of th
is a process parameter that depends on the size of the wafer
type of resist used. The amount of resist deposited in the puddl

heated to the vapor point and the wafers are suspended in the vapors for coating.

A newer technique is vacuum vapor priming, which uses a sealed flask of HMDS connected to a vacuum oven or single-wafer chamber. The wafers are first heated in the oven in a nitrogen atmosphere. After a temperature of about 150°C is reached, the atmosphere is switched to a vacuum. Once the vacuum level is reached, a valve is opened and HMDS vapors are drawn into the chamber by the low pressure. Within the chamber, the wafers become completely coated as the vapors fill the entire chamber. This method has shown good adhesion longevity even in the presence of high humidity.[6]

Vacuum vapor priming offers the additional advantage of a combined dehydration bake and prime step and a significant reduction in HMDS usage. In a production area that typically uses gallons of HMDS per week, switching to vacuum vapor priming will reduce usage to pints per month. Vacuum vapor priming practiced in a chest-type oven adds an additional step to the process. Many automatic spinner systems offer in-line vapor primers.

Photoresist spinning

The purpose of the photoresist application step is the establishment of a thin, uniform, defect-free film of photoresist on the wafer surface. These qualities are easy to state, but they require sophisticated equipment and stringent controls to achieve. A typical resist layer varies from 0.5 to 1.5 μm in thickness and has to have a uniformity of plus or minus only 0.01 μm (100 Å). This variation is 1 percent of a 1.0-μm thickness.

The usual methods of applying thin layers of liquids to surfaces are brushing, rolling, and dipping. None of these methods is adequate to achieve the quality resist film necessary for photomasking. The method used is spinning, which was briefly described in the section on priming. Spinners are built in manual, semiautomatic, and automatic designs. The systems differ in the degree of automation and are described in the following text. However, the deposit of the film on the wafer is common to each of the systems.

The static spin process. The wafer that is ready for spinning (after priming) is on the vacuum chuck. Several cubic centimeters (cm^3) of the photoresist is deposited in the center of the wafer (Fig. 8.28) and allowed to spread out into a puddle. The puddle is allowed to spread until it covers the majority of the wafer surface. The size of the puddle is a process parameter that depends on the size of the wafer and the type of resist used. The amount of resist deposited in the puddle is crit-

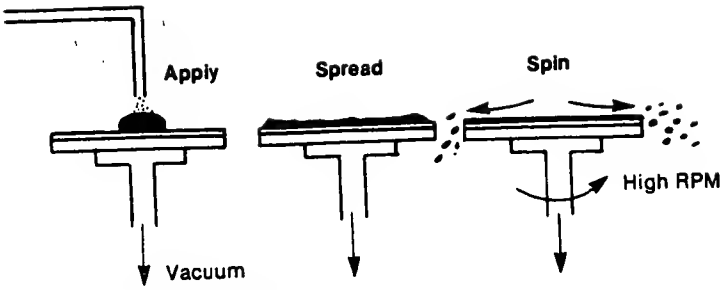

Figure 8.28 Static spin process.

ical only in the extremes. Too small an amount will result in incomplete resist coverage, and too much will cause a buildup of a resist rim or result in resist on the back of the wafer (Fig. 8.29).

When the puddle reaches its specified diameter, the chuck is rapidly accelerated to a predetermined speed. During the acceleration, centrifugal forces spread the resist to the wafer edge and throw off excess resist, leaving a thin uniform layer on the wafer. The high-speed spin continues for some time after the resist is spread to allow drying of the resist.

The final thickness of the film is established as the result of the resist viscosity, the spin speed, the surface tension, and the drying characteristics of the resist. In practice, surface tension and the drying characteristics are properties of the resist, and the viscosity–spin

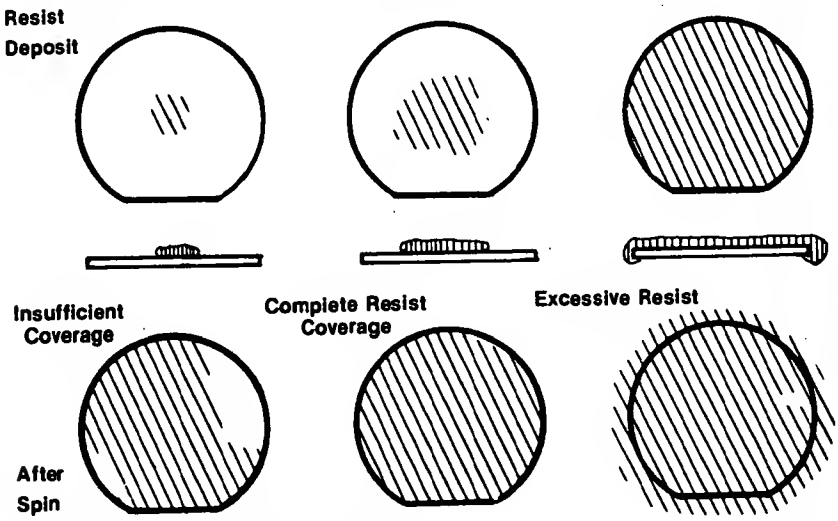

Figure 8.29 Example of resist coverage.

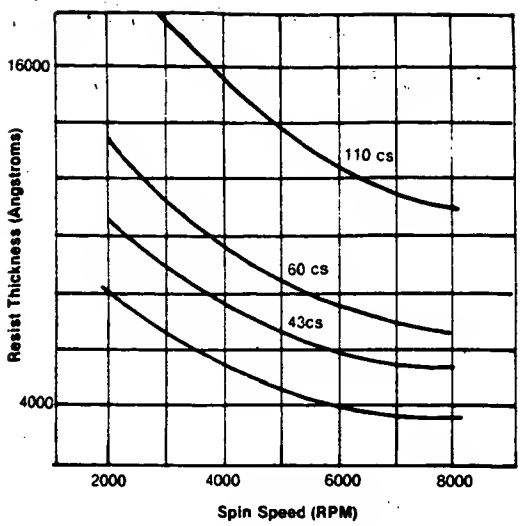

Figure 8.30 Resist thickness versus spin speed. (*Courtesy of KTI Chemicals.*)

speed relationship is determined from curves supplied by the resist manufacturer or established for the particular spin system used (Fig. 8.30).

Although spin speed is specified to control resist thickness, it is actually the acceleration rate that establishes the final resist thickness. The acceleration characteristic of the spinner must be specified, and it is usually maintained as a constant in the spin process.

Dynamic dispense. The need for uniform resist films on larger-diameter wafers led to the development of the dynamic spin dispensing technique in the 1970s (Fig. 8.31). For this technique the wafer is rotated at a low speed of approximately 500 rpm. While the wafer is rotating, the resist is dispensed onto the surface. The action of the rotation assists in the initial spreading of the resist. Less resist is used and a more uniform layer is achieved. After spreading of the resist, the spinner is accelerated to a high speed to complete the spread and thin the resist into a uniform film.

Moving-arm dispensing. An improvement on the dynamic dispense technique is the addition of a moving-arm resist dispenser (Fig. 8.32). The arm moves in a slow motion from the center of the wafer toward its edge. This action creates more uniform initial and final layers. A moving-arm dispenser also saves resist material, especially for larger-diameter wafers.

Batch Number	Broken Wafer	Scratch	Contamination	Pinholes	MA	Bridging	Lifting Resist	Under Exposed	Incomplete Develop	No Resist	Resist Running	Wrong Mask	C.D.	Reject

Figure 9.13 Typical develop inspect log.

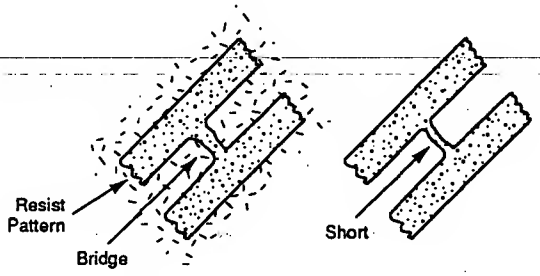

Figure 9.14 Bridged conduction lines.

from an overexposure, poor mask definition, or a resist film that is too thick.

Etch

At the completion of the develop inspect step, the mask (or reticle) pattern is defined in the photoresist layer and is ready for etch. During the etch step the image will be permanently transferred into the surface layer on the wafer. The goal is an exact transfer of the image into the resist layer. The degree of exactness is dependent on several factors which will be explored as a preparation for discussion of the dif-

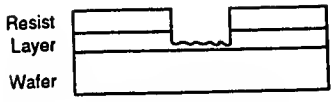

Figure 9.15 Incomplete etch.

ferent etch methods. The factors affecting image transfer are incomplete etch, overetching, undercutting, and selectivity.

Incomplete etch

Incomplete etch is a situation in which a portion of the surface layer still remains in the pattern hole or on the surface (Fig. 9.15). The causes of incomplete etch are too short an etch time, the presence of a surface layer that slows the etching, or an uneven surface layer that results in incomplete etch in the more thickly coated portions of the wafer. If wet-chemical etching is used, a lowered temperature or weak etch solution will cause incomplete etch. If dry plasma etching is used, a wrong gas mixture or an improperly operated system can cause the same effect.

Overetch and undercutting

The opposite condition to incomplete etch is overetch. In any etch process there is always some degree of overetch planned into the process. This is necessary to ensure complete removal of the thickest portions of the the layer and to allow for the etch to break through any slow-etching layers on the top surface.

The ideal etch leaves vertical sidewalls in the layer (Fig. 9.16). Etch techniques that produce this ideal result are said to be *anisotropic*. However, the etching chemical dissolves the top of the sidewall for a longer time than the bottom of the hole. The result is a hole wider at the top than the bottom with a sloped sidewall. Etching techniques that produce this result are called *isotropic*. This action of the etching chemical is called *undercutting* (Fig. 9.17) since the surface layer is undercut below the resist edge. Circuit layout designers take undercutting into account when planning the circuit. Adjacent patterns must be separated a certain distance to prevent shorting. The amount of undercutting must be calculated when the pattern is designed.

An ongoing goal of the etch step is the control of undercutting to an acceptable level. Severe undercutting (or overetch) takes place when the etch time is excessive, the etch temperature is too high, or the etch mixture is too strong. Undercutting is also present when the adhesion bond between the photoresist and the wafer surface is weak. This is a constant worry, and the purpose of the dehydration, prime, soft bake,

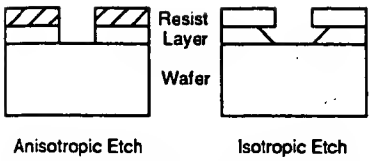

Figure 9.16 Anisotropic and isotropic etch.

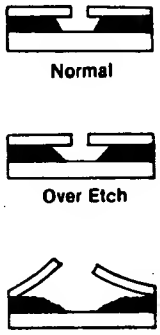

Figure 9.17 Degrees of undercutting.

and hard bake steps is to prevent this type of failure. Failure of the resist bond at the edge of the etch hole can result in severe undercutting. If the bond is very poor, the resist can lift from the wafer surface, causing catastrophic undercutting.

Selectivity

Another goal of the etch step is the preservation of the surface underlying the etched layer. If the underlying surface of the wafer is partially etched away, the physical dimensions and electrical performance of the devices are changed. The property of the etch process that relates to preservation of the surface is *selectivity*. High selectivity implies little or no attack of the underlying surface. In wet etching techniques an etchant acid that will not attack the underlying material is chosen.

Wet Etching

For over 30 years the traditional method of etching has been by immersion techniques using wet etchants. The procedure is similar to the preoxidation clean-rinse-dry process (Chap. 7) and immersion development. The emergence of feature sizes less than 3 μm has seen the shift from wet to dry etching techniques. However, keep in mind that within a circuit whose smallest dimensions are 3 μm or less, there are still mask levels with dimensions well above that level. In many cases dry etching is employed for small dimensions and wet etching for the larger ones.

For wet etching, the wafers are loaded into an etch-resistant boat and immersed in a tank of the etchant. After a predetermined time in the etch tank they are processed through the rinsing and drying steps.

Etching uniformity and process control are enhanced by the addition of heaters and agitation devices, such as stirrers or ultrasonic waves, to the immersion tanks.

Although the basic equipment is simple in concept, a high-production wet "bench" can be very sophisticated,[9] incorporating microprocessor control of the timers and heaters. Many systems have walking beams or robots for the automatic placement of the wafer holders in the etch, rinse, and dry subsystems. The etch tanks of the traditional manual systems are filled by hand, a dangerous and possibly contaminating practice. Newer systems have plumbing to allow the filling of the tanks from reserve tanks by remote control.

The worry about etchant contamination of the wafers is being addressed by *point-of-use filters*. These are special filters fitted to automatic chemical dispensing systems to filter-clean the chemicals just prior to filling the immersion tank. This placement catches particulate contamination from the chemicals, the pumps, and the tubing systems.

Wet etchants are selected for their ability to uniformly remove the top wafer layer without attacking the underlying material (good selectivity).

Etch time variability is introduced by temperature variations as the boat and wafers come to temperature equilibrium in the tank and the continued etching action as the wafers are transferred to a rinse tank. Generally, the process is set at the shortest time compatible with uniform etching and high productivity. The maximum time is limited to the amount of time the resist will continue to adhere to the wafer surface.

Silicon wet etching

Silicon layers are typically etched with a solution of nitric and HF acids mixed in water. The formula becomes an important factor in control of the etch. In some ratios, the etch has an exothermic reaction with the silicon. Exothermic reactions are those that produce heat, which, in turn, speeds up the etch reaction, which, in turn, creates more heat, and so on, resulting in an uncontrollable process. Sometimes acetic acid is mixed in with the other ingredients to control the exothermic reaction.

Some devices require the etching of a trough or trench into the silicon surface. The etch formula is adjusted to make the etch rate dependent on the orientation of the wafer. ⟨111⟩-oriented wafers etch at a 45° angle, while ⟨100⟩-oriented wafers etch with a "flat" bottom.[3]

Other orientations result in different-shaped trenches. Polysilicon films are also etched with the same basic formula.

Silicon dioxide wet etching

The most common etched layer is a thermally grown silicon dioxide. The basic etchant is hydrofluoric acid (HF). HF has the advantage of dissolving silicon dioxide without attacking silicon. However, full-strength HF has an etch rate of about 300 Å/s at room temperature.[4] This rate is too fast for a controllable process (a 3000-Å layer would etch in only 10 s).

In practice, the HF (assay of 49%) is mixed with water or ammonium fluoride and water. The ammonium fluoride (NH_4F) acts as a buffer to the unwanted generation of hydrogen ions which accelerate the etch rate. These solutions are known as *buffered oxide etches* or BOEs. They are mixed in different strengths to create reasonable etch times for the particular oxide thickness (Fig. 9.18). Some BOE formulas include a wetting agent (surfactant such as Triton X-100 or equivalent) to reduce the surface tension of the etch, allowing it to uniformly penetrate into smaller openings.

Aluminum film wet etching

Selective etching solutions for aluminum and aluminum alloy layers are based on phosphoric acid. An unfortunate by-product of the reaction of aluminum and phosphoric acid are tiny bubbles of hydrogen, as

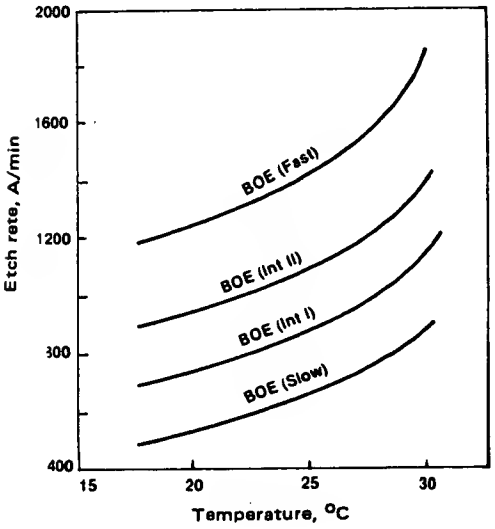

Figure 9.18 Etch rate versus temperature for BOEs.

shown in the reaction in Fig. 9.19. These bubbles cling to the wafer surface and block the etch action. The result is either bridges of aluminum that can cause electrical shorts between adjacent leads or spots of unwanted aluminum, called *snowballs*, left on the surface. Neutralization of this problem is accomplished by use of an aluminum etching solution that contains phosphoric acid, nitric acid, acetic acid, water, and wetting agents. A typical solution of the active ingredients (less wetting agent) is 16:1:1:2.

In addition to the special formulas, a typical aluminum etch process will include wafer agitation by stirring or moving the wafer boat up and down in the solution. Sometimes ultrasonic or megasonic waves are used to collapse and move the bubbles around.

Deposited oxide wet etching

One of the final layers on a wafer is a silicon dioxide passivation film deposited over the aluminum metallization pattern. These films are known as vapox or silox films. While the chemical composition of the films is that of silicon dioxide, the same as thermally grown silicon dioxide, they require a different etch solution. The difference is in the selectivity required of the etchant.

The usual etchant for silicon dioxide is a BOE solution. Unfortunately, the BOE attacks the underlying aluminum pads, causing bonding problems in the packaging process. This condition is called *brown*, or *stained, pads*. The preferred etchant for this layer is a solution of ammonium fluoride and acetic acid mixed in a ratio of 1:2.

Silicon nitride wet etching

Another compound favored for the passivation layer is silicon nitride. It is possible to etch this layer with wet chemical means, but it is not as easy as for the other layers. The chemical used is hot (180°C) phos-

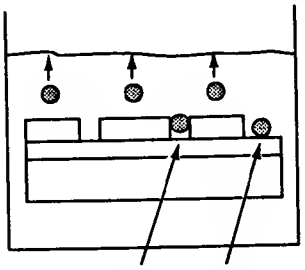

Figure 9.19 Hydrogen bubble blockage of etchant.

	COMMON ETCHANT	ETCH TEMP	RATE Å /MIN	METHOD
SiO_2	HF & NH_4F (1 : 8)	Room	700	Dip & wetting agent predip
SiO_2	HF & NH_4F (1 : 8)	Room	700	Dip & wetting agent predip
SiO_2 (Vapox)	Acetic Acid & NH_4F(2 : 1)	Room	1000	Dip
Aluminum	H_3PO_4 : 16 HNO_3 : 1 Acetic : 1 H_2O : 2 Wetting Agent	40 - 50°C	2000	a) Dip & agitation b) Spray
Si_3N_4	H_3PO_4	150 - 180°C	80	Dip
POLYSi	HNO_3 : 50 H_2O : 20 HF : 3	Room	1000	Dip

Figure 9.20 Summary of wet etching process.

phoric acid. Since the acid evaporates rapidly at this temperature, the etch must be done in a closed reflux container equipped with a cooled lid to condense the vapors. The major problem is that photoresist layers do not stand up to the etchant temperature and aggressive etch rate. Consequently, a layer of silicon dioxide or some other material is required to block the etchant. These two factors have led to the use of dry etching techniques for silicon nitride.

Wet spray etching

Wet spray etching offers several advantages over immersion etching. Primary is the added definition gained from the mechanical pressure of the spray.[5] Spray etching also minimizes contamination from the etchants. From a process control point of view, spray etch is more controllable since the etchant can be instantly removed from the surface by switching the system to a water rinse. Single-wafer spinning-chuck spray systems offer considerable process uniformity advantages.

Disadvantages to spray etching are system cost, safety considerations associated with caustic etchants in a pressurized system, and the requirement of etch-resistant materials to prevent the deterioration of the machine. On the plus side, spray systems are usually enclosed, which adds to worker safety. Figure 9.20 is a table of common semiconductor films and their common etchants.

Dry Etch

The limits of wet etching for VLSI-size patterns has been mentioned in the previous section. For review they are

1. Wet etching is limited to pattern sizes of 3 μm.
2. Wet etching is isotropic, resulting in sloped sidewalls.
3. A wet etch process requires rinse and dry steps.
4. The wet chemicals are hazardous and/or toxic.
5. Wet processes represent a contamination potential.
6. Failure of the resist-wafer bond causes undercutting.

These considerations have led to the use of dry etch processes for the definition of small feature sizes on advanced circuits. Figure 9.21 is an overview of the dry etching techniques used.

Dry etching is a generic term that refers to the etching techniques in which gases are the primary etch medium, and the wafers are etched without wet chemicals or rinsing. The wafers enter and exit the system in a dry state.

Barrel plasma etching

The term dry etching is sometimes used to refer to plasma etching, although there are two other dry etching techniques—ion milling and reactive ion etch. Plasma etching, like wet etching, is a chemical process but uses plasma energy to drive the reaction. Comparison of silicon dioxide etching in the two systems illustrates the differences. In wet etching of silicon dioxide, the fluorine in the BOE etchant is the ingredient that dissolves the silicon dioxide, converting it to water-rinsable components. The energy required to drive the reaction comes from the internal energy in the BOE solution or from an external heater.

A plasma etcher requires the same elements: a chemical etchant and an energy source. Physically, a plasma etcher consists of a chamber, vacuum system, gas supply, and a power supply (Fig. 9.22). The wafers are loaded into the chamber and the pressure inside is reduced

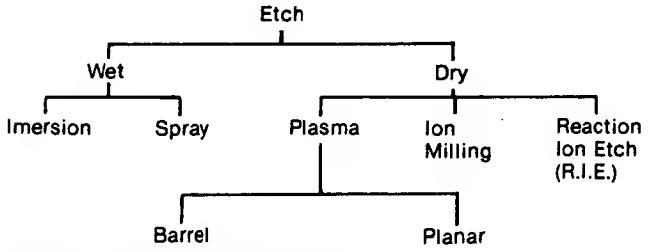

Figure 9.21 Guide to etch methods.

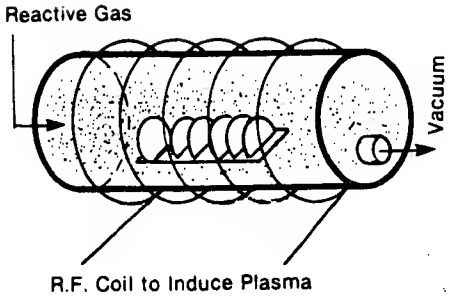

Figure 9.22 Barrel plasma etch.

by the vacuum system. After the vacuum is established, the chamber is filled with the reactive gas. For the etching of silicon dioxide the gas is usually CF_4 mixed with oxygen. The power supply creates a radiofrequency (RF) field through electrodes in the chamber. The field energizes the gas mixture to a plasma state. In the energized state the fluorine attacks the silicon dioxide, converting it into volatile components that are removed from the system by the vacuum system.

The earlier plasma systems were designed with circular chambers and are called *barrel etchers*. While providing the benefits of dry etching, barrel plasma systems produce isotropic etching. Within the chamber the etching ions are energized by the plasma in a nondirectional manner. The etching ions attack the surface layer from all directions, creating a tapered sidewall. In a barrel system, the wafers are held in a boat and etching relies on the mixing of the etching ions between the wafers. Uniform etching of wafers in a barrel etching system is difficult because it is hard to supply a constant amount of etchant to all the wafers in the system and because of the nondirectionality of the etching ions.

Another consideration of barrel plasma etching is radiation damage resulting from the high-energy plasma field. The high energy causes charges to build up in the wafer surface that compromise the electrical functioning of the circuit. Protection of the wafers from the radiation is provided by perforated metal cylinders that isolate the wafers from the plasma field (Fig. 9.23).

Planar plasma etching

For more precise etching, plasma planar systems are preferred. These systems contain the basic elements of the barrel system, but the wafers are placed on a grounded pallet under the RF electrode (Fig. 9.24). The wafers are actually in the plasma field and the etching ions are more directional than those in a barrel system. The result is a more

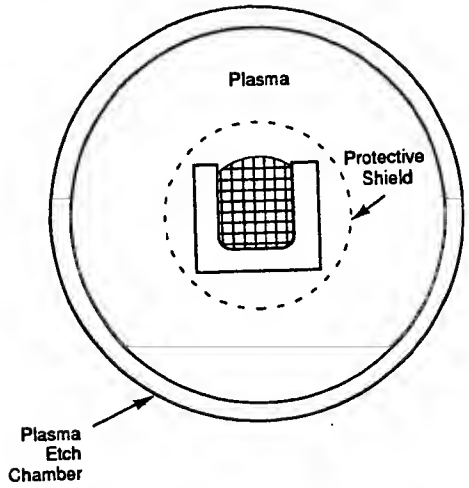

Figure 9.23 Barrel plasma stripper with protective shield.

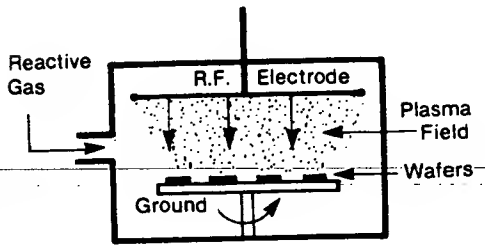

Figure 9.24 Planar plasma etch.

anisotropic etch with almost vertical sidewalls possible. Etching uniformity is increased with the rotation of the wafer pallet in the system.

Etching of silicon dioxide in a planar system takes place in C_4F_8, which provides good selectivity when etching silicon dioxide over silicon substrates. Selectivity is a major consideration of plasma etching processes. The three methods used to control selectivity are the selection of the etching gas formula, the dilution of the gas near the end of the process to slow down the attack of the underlying layer, and endpoint detectors in the system. An endpoint detector for a silicon dioxide etch over silicon would automatically terminate the etching process as soon as some silicon was detected in the exiting gas stream.

The etch rate of a plasma system is determined by the power supplied to the electrodes, the chemistry of the gas etchants (Fig. 9.25), and the vacuum (pressure) level in the chamber. Etch rates vary from 600 to 2000 Å/min.[6] Planar plasma etch systems are designed in both batch and single-wafer chamber configurations. The single-wafer systems are popular for their ability to have the etch parameters tightly

Film	Etchant	Typical Gas Compounds
Al	Chlorine	$BCl_3, CCl_4, Cl_2, SiCl_4$
Mo	Fluorine	CF_4, SF_4, SF_6
Polymers	Oxygen CF_4, SF_4, SF_6	
Si	Chlorine, Fluorine CF_4, SF_4, SF_6	$BCl_3, CCl_4, Cl_2, SiCl_4$
SiO_2	Chlorine, Fluorine	$CF_4, CHF_3, C_2F_6, C_3F_8$
Ta	Fluorine	"
Ti	Chlorine, Fluorine	"
W	Fluorine	"

Figure 9.25 Plasma etch chemicals.

controlled for uniform etching. Also, with load-lock chambers single-wafer systems can maintain high production rates and are amenable to in-line automation.

Ion beam etching

A second type of dry etch system is the ion beam system (Fig. 9.26). Unlike plasma systems, ion beam etching is a physical process. The

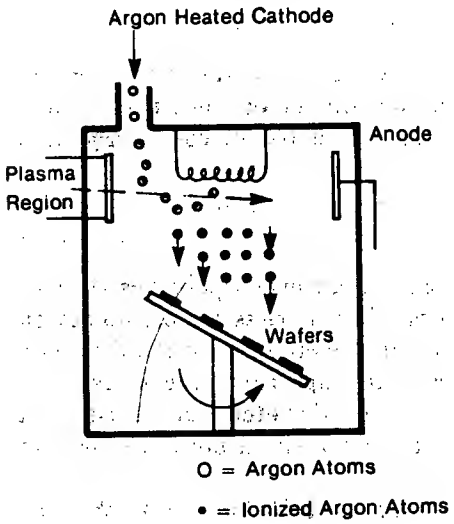

Figure 9.26 Ion beam milling.

wafers are placed on a holder in a vacuum chamber and a stream of argon is introduced into the chamber. Upon entering the chamber, the argon is subjected to a stream of high-energy electrons from a set of cathode-anode electrodes. The electrons ionize the argon atoms to a high-energy state with a positive charge. The wafers are held on a negatively grounded holder which attracts the ionized argon atoms. As the argon atoms travel to the wafer holder they accelerate, picking up energy. At the wafer surface they crash into the exposed wafer layer and literally blast small amounts from the wafer surface. Scientists call this action a *momentum transfer*, a physical process. No chemical reaction takes place between the argon atoms and the wafer material. Ion beam etching is also called *sputter etching* or *ion milling*.

The material removal (etching) is highly directional, resulting in good definition of small openings. Two considerations of ion beam etching is its poor selectivity and radiation damage from the ionization mechanism.

Reactive ion etching

Reactive ion etching (RIE) systems combine plasma etching and ion beam etching principles. The systems are similar in construction to the plasma and the ion beam systems but have a capability of ion milling. The combination brings the benefits of chemical plasma etching along with the benefits of directional ion milling. A major advantage of RIE systems is in the etching of silicon dioxide over silicon layers. The combination etch results in a selectivity ratio of 35:1,[7] whereas ratios of only 10:1 are available with plasma-only etching.

Dry etch etchants

As in wet etching, the selection of a dry etchant is dependent on the layer to be etched, the material under the layer, and the etching method selected. The table in Fig. 9.25 is a list of commonly used etchant gases.

Resist etch barriers in dry etching

For both wet and dry etching processes, a patterned photoresist layer is the preferred etch barrier. In wet etching there is almost no attack of the resist by the etchants. However, in dry etching, residual oxygen in the system attacks the resist layer. An important process parameter is the thickness of a resist destined for a dry etch. The resist must be thick enough to stand up to the etchants without becoming so thin that pinholes are present.

Another resist-related dry etch problem is resist baking. Within the

dry etch chamber, the temperature can rise as high as 200°C, a temperature that can bake the resist to a condition that makes it hard to remove from the wafer. Another temperature-related problem is the tendency of resist patterns to flow and distort the images.

Resist Stripping

After etching, the pattern is a permanent part of the top layer of the wafer. The resist layer that has acted as an etch barrier is no longer needed after etching and is removed (or stripped) from the surface. Traditionally, the resist layer has been removed by wet chemical processing. The development of dry etching systems has led to the use of plasma stripping.

Wet chemical stripping of nonmetal surfaces

A number of different chemicals are used for stripping. The choice depends on the wafer surface the resist is being removed from, production considerations, and the polarity of the resist (Fig. 9.27). Generally the strippers are divided into the categories of universal strippers and positive- and negative-only strippers.

Wet stripping is favored for the following reasons:

1. It has a long process history.
2. It is cost-effective.
3. It is effective in the removal of metallic ions.
4. It is a low-temperature process and does not expose the wafers to possibly damaging radiation.

A wet stripping process requires the same steps as a wet etch: strip, water rinse, and dry.

Sulfuric acid and hydrogen peroxide. Solutions of sulfuric acid and hydrogen peroxide are the most common strippers used for the removal

Stripper	Operating Temperature	Oxide	Surface Metalized	Bathlife	Resist Polarity		REMOVAL
					Negative	Positive	
1) Sulfuric Acid & Oxidant	125°C	X		2-3 Hrs	X	X	Neutralize
a. exothermic							
b. heated	↓	X		8 Hrs	X	X	Neutralize
2) Organic Acids	90-110°C	X	X	4-8 Hrs	X	X	Remove & bury
3) Chromic/Sulfuric Acid mixture	20°C	X	X	4-8 Hrs	X	X	Remove & bury
4) Solvents	20°C-90°C	X	X	4-8 Hrs	X	X	Remove & recycle

Figure 9.27 Comparison of wet photoresist strippers.

Chemical-mechanical planarization

From Wikipedia, the free encyclopedia.
(Redirected from Chemical mechanical polish)

Chemical-mechanical planarization or **Chemical-mechanical polishing**, commonly abbreviated **CMP**, is a technique used in semiconductor fabrication for planarizing the top surface of an in-process semiconductor wafer or other substrate.

The process uses an abrasive and corrosive chemical slurry (commonly a colloid) in conjunction with a polishing pad, typically of a greater diameter than the wafer. The pad and wafer are pressed together and rotated at different rates, with different axes of rotation (i.e., not concentric). This removes material and tends to even out any irregular topography, making the wafer flat or planar. This may be necessary in order to set up the wafer for the formation of additional circuit elements. For example, this might be necessary in order to bring the entire surface within the depth of field of a photolithography system, or to selectively remove material based on its position.

The process of material removal is not simply that of abrasive scraping, like sandpaper on wood. The chemicals in the slurry also react with and/or weaken the material to be removed. The abrasive accelerates this weakening process and the polishing pad helps to wipe the reacted materials from the surface. The process has been likened to that of a child eating a gummy candy. If the candy sits on the tongue without being scraped around, the candy becomes covered with a gel coating, but the majority of the candy is not affected. Only with a vigourous scraping does the candy dissolve away.

Before about 1994 CMP was looked on as too "dirty" to be included in high-precision fabrication processes, since abrasion tends to create particles and the abrasives themselves are not without impuritites. Since that time, the integrated circuit industry has moved from aluminium to copper conductors. This required the development of an *additive patterning* process, which relies on the unique abilities of CMP to remove material in a planar and uniform fashion and to stop repeatably at the interface between copper and oxide insulating layers (see Copper-based chips for details). Adoption of this process has made CMP processing much more widespread.

Retrieved from "http://en.wikipedia.org/wiki/Chemical-mechanical_planarization"

Categories: Technology stubs | Semiconductor device fabrication | Chemical processes

SILICON PROCESSING

FOR

THE VLSI ERA

VOLUME 2:

PROCESS INTEGRATION

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properties of ECR silicon-oxide and silicon-nitride films are given in references 103, 104, and 105.

It has been observed that the physical properties of the ECR films are better than those obtained with conventional PECVD processes. However, the step coverage can be very nonconformal, and the sidewall films can be quite porous if the film is deposited without rf bias.

Films deposited in conventional ECR machines exhibit non-uniform thickness, especially on large wafers (≥150 mm), due to the divergent magnetic field that extracts the ions from the microwave cavity. The modified magnetic coils of more recently designed machines make it possible to produce films with ±5% thickness uniformities across 150-mm wafers.[106]

A system that uses ECR to generate a plasma with oxygen gas (instead of Ar) has been reported for sputtering layers of SiO_2 by formed CVD in the same chamber.[261] The oxygen ions sputter the SiO_2 (formed earlier by reaction of SiH_4 and O_2) to achieve planarization. This can be achieved without applying a dc bias the substrate or by having self-bias develop between the wafer and the plasma. That is, an rf signal at 400 kHz is applied to the substrate. The impinging oxygen ions from the plasma can follow this electric field, and thus bombard the surface without having a self-bias build up on the substrate. Electrostatically-caused damage (due to the buildup of charge on the wafer surface as a result of self-bias) is thus prevented, while the sputtering needed to achieve planarization still occurs. High sputtering rates of SiO_2 films with low damage have been reported.

4.4.11 Chemical-Mechanical Polishing

The sacrificial-resist etchback process, even with a compensated-PBM resist layer, still has severe problems for multilevel metal applications. The deposition and etchback tolerances associated with large film thicknesses are cumulative, and any non-planarity of the resist is replicated in the final planarized oxide surface. Under RIE etchback conditions designed to reduce such non-planarities (i.e., the oxide/resist etchrate ratio is increased to more than 1.0), oxide spikes are caused (Fig. 4-35a). A chemical-mechanical polishing (CMP) process has recently been reported for removing such spikes.[265] The CMP process can rapidly remove such small elevated features without significantly thinning the oxide on the flat areas (Fig. 4-35b). It is pointed out that the CMP process alone is not viable for planarization because residual oxide will be left in the middle of large active areas or arrays after polishing (Fig. 4-35c). By using CMP and etchback planarization, however, an effective planarization method can be achieved.

Not many details about CMP technology have been published as of this writing, but references to silicon wafer-polishing techniques have been cited.[266] To prevent mechanical work damage from remaining on the polished film, the chemical component of the polishing should probably dominate. Since the wafers will likely be polished one at a time, the throughput is also likely to be low (e.g., on the order of 5-10 wafers per hour). Other predicted problems include the clean-up of the polishing-slurry particles from the wafer surface (slurry-particle size <0.1 μm), the question of how to make

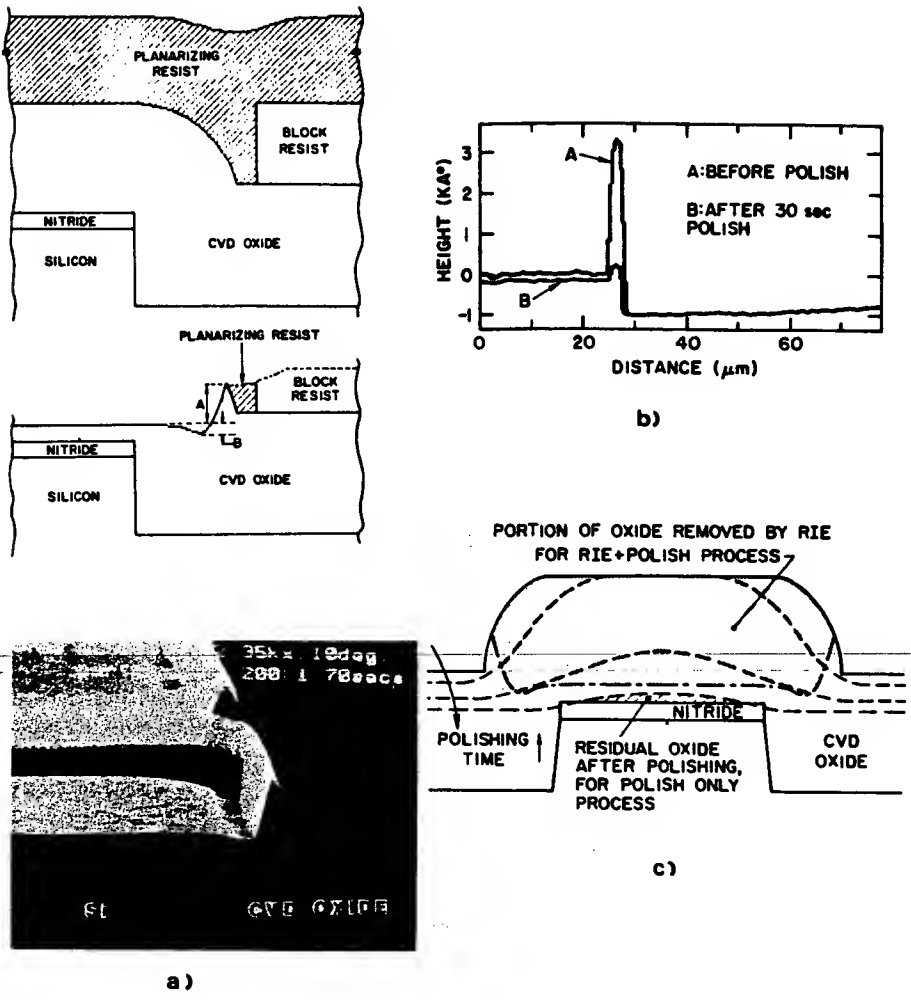

Fig. 4-35 (a) Cross section after selective RIE etchback, showing local oxide spikes that remain after the etchback when the oxide/resist etch-rate ratio > 1. (b) Measured oxide step heights before and after CMP, showing the fast removal rate of such spikes. (c) Schematic drawing showing the fundamental problem of "CMP-only" planarization.[264] (© 1989 IEEE).

such a dirty process compatible with the clean room environment (i.e., reducing the density of the 50,000 to 100,000 particles/ft^3 generated, to less than 50/ft^3), the lack of an end point detection method, and maintaining sufficient polishing-rate uniformity across the wafer, and from wafer to wafer. Commercially available equipment for performing this process is reportedly being developed.

SILICON PROCESSING FOR THE VLSI ERA

VOLUME 1:

PROCESS TECHNOLOGY

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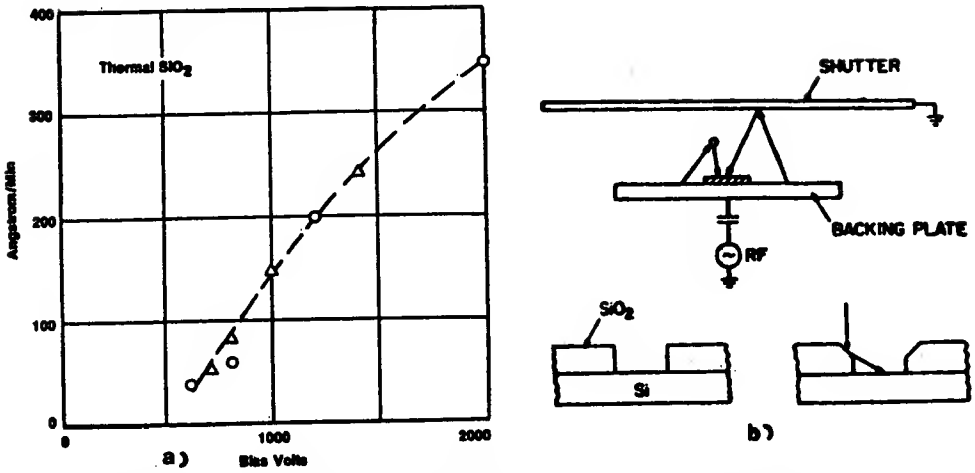

Fig. 4 (a) Example of sputter-etch rate of thermal SiO_2. Courtesy of Varian Associates. Contamination of contacts during sputter etching by (b) backscattering events, and (c) faceting. Material sputtered from the facet deposits in the contact at a rate that can exceed removal of material from the bottom of the opening[10]. Reprinted by permission of the American Physical Soc.

(2000-3000 lb /in^2) DI water jet sweeps across the wafer surface and removes the microscopic debris dislodged by the brush, as well as any residual particles generated by the brush.

In-Situ Sputter Etch Removal of Native Oxide Films

A thin oxide (5-50 Å) grows on silicon (SiO_2) or aluminum (Al_2O_3) when these materials are exposed to air. This thin oxide (known as *native oxide*) can adversely effect subsequent processing steps, for example by causing high contact resistance, or impeding interfacial reactions of films deposited on the substrate materials. Thus, it is important to remove this oxide layer and keep it from reforming before depositing the overlying film.

Concerns have arisen about whether chemical cleaning techniques will be adequate for removing native oxide films, especially in contact holes or via regions smaller than 2 μm. As a result removal of such films is also being conducted in the same vacuum environment in which the overlying film will be deposited (*in situ*). Sputter etching is used to remove up to several hundred angstroms of the wafer surface including, it is surmised, the unwanted native oxide at the bottom of the contacts or vias. Some questions have also been raised about the effectiveness of this technique for small (e.g. < 2 μm) contacts[10]. It is argued that such sputter etching (Fig. 4) will cause more contamination of the contacts through redeposition by backscattering of material sputtered from wafers and chamber surfaces, and by sputtering of contact sidewall material into the contact bottom. *In situ* removal of the native oxide by plasma chemical reactions, instead of physical sputtering mechanisms, has been proposed to circumvent this problem. Several sputter equipment suppliers offer such alternative *in situ* cleaning capabilities.

TERMINOLOGY OF ETCHING

Etching in microelectronic fabrication is a process by which material is removed from the silicon substrate or from thin films on the substrate surface. When a *mask layer* is used to protect specific regions of the wafer surface, the goal of etching is to precisely remove the

material which is not covered by the mask (Fig. 5). In this section we will discuss the terms used to describe the basic aspects of etch processes.

Bias, Tolerance, Etch Rate, and Anisotropy

In general an ideal etch process is not completely attainable. That is, the etching processes are not capable of precisely transferring the pattern established by the protective mask into the underlying material. The degree to which the process fails to satisfy the ideal is specified by two parameters: *bias* and *tolerance*. As shown in Fig. 6d, *bias* is the difference in lateral dimension between the etched image and the mask image. *Tolerance* is a measure of the statistical distribution of bias values that characterizes the uniformity of etching. The tolerance parameter can be specified for a single wafer (bias distribution across a wafer), for an entire lot (bias distribution throughout the lot) or from run-to-run (bias distribution across a group of runs).

The rate at which material is removed from the film by etching is known as the *etch rate*. The units of etch rate are typically expressed in Å /sec, μm /min, etc. Generally, high etch rates are desirable as they allow higher production throughputs, but in some cases high etch rates make control of lateral etching a problem. That is, since material removal can occur in both the horizontal and vertical directions, the *horizontal etch rate* as well as the *vertical etch rate* may need to be established in order to characterize an etch process. Normally the uniformity of these etch rates is also of interest, and is expressed for three conditions (across a wafer, from wafer-to-wafer, and from run-to-run), as *etch rate % uniformity*, according to:

$$\text{Etch Rate Percent Uniformity} = \frac{(\text{Etch Rate}_{high} - \text{Etch Rate}_{low})}{(\text{Etch Rate}_{high} + \text{Etch Rate}_{low})} \times 100\% \qquad (1)$$

Highly uniform etch rates are almost always desirable in an etch process.

The lateral etch ratio, L_R, is defined as the ratio of the etch rate in a horizontal direction to

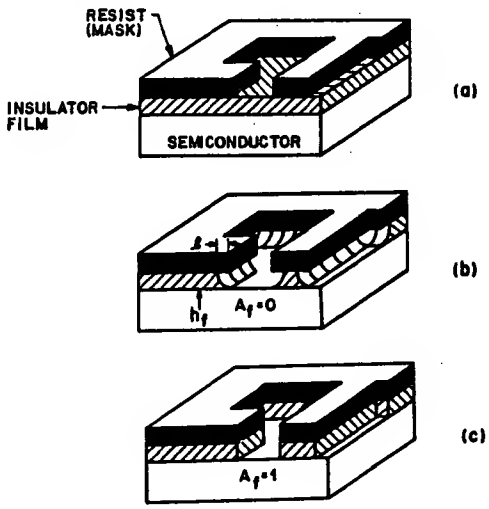

Fig. 5 Comparison of (b) isotropic, and (c) completely anisotropic etching. From E.C. Douglas, *Solid State Tehnol.*, 24, 65, (1981). Reprinted with permission of Solid State Technology, published by Technical Publishing, a company of Dun & Bradstreet.

that in the vertical direction. Thus:

$$L_R = \frac{\text{Horizontal Etch Rate of Material}}{\text{Vertical Etch Rate of Material}} \quad (2)$$

In the case of an ideal etch process the mask pattern would be transferred to the underlying layer with zero bias. This would then create a vertical edge profile in the etched layer coincident with original edge of the mask. Therefore the lateral etch rate would also have to have been zero. For non-zero L_R, the film material is etched to some degree under the mask and this effect is called *undercut* (Fig. 5d).

When the etching can proceed in all directions at the same rate, it is said to be *isotropic* (Fig. 5b). By definition, however, any etching that is not isotropic is *anisotropic*. If etching proceeds exclusively in one direction (e.g. only vertically), the etching process is said to be *completely anisotropic*. Since many etch processes fall between the extremes of being isotropic and completely anisotropic, it is useful to define a degree of anisotropy, A, as:

$$A = 1 - L_R \quad (3)$$

Thus, when $L_R = 0$, $A = 1$, and this condition corresponds to completely anisotropic etching. When $L_R = 1$, the vertical and horizontal etch rates are equal, and the degree of anisotropy is $A = 0$. This corresponds to an isotropic etching condition. Most wet etching processes and some dry-etching processes exhibit uniform etch rates in all directions, and hence are isotropic.

An example of an etch profile in the film being removed versus time is shown for an isotropic etch, $L_R = 1$ (Fig. 6a) and for a process in which $L_R = 0.1$ (Fig. 6b). If the films are etched just to completion, the profile for $L_R = 1$ has the shape of a quarter circle, whereas the profile of $L_R = 0.1$ is vertical except near the bottom (where it is rounded). If this etch is allowed to continue, however, even the profile with $L_R = 1$ becomes more vertical, though

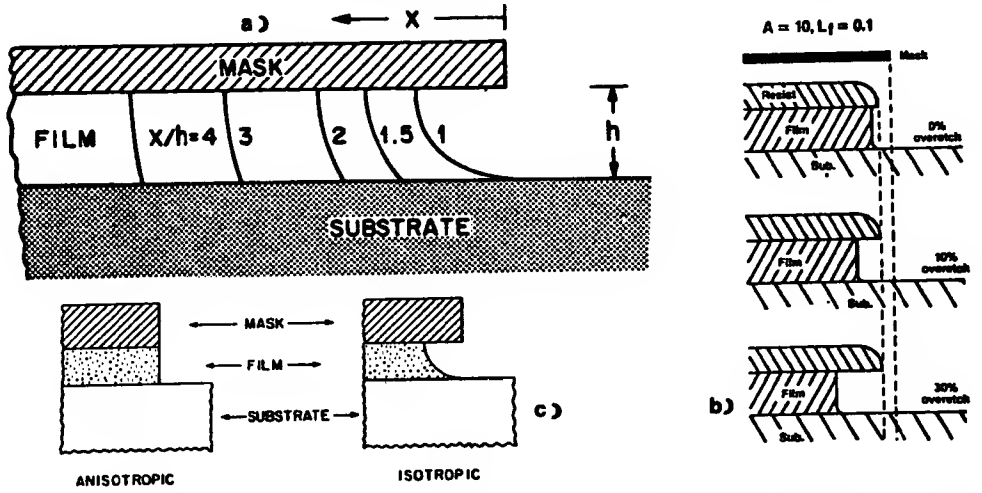

Fig. 6 (a) Isotropic etching of a film vs time ($L_R = 1$). Overetching results in profiles are more vertical. (b) Etching of film versus time when $L_R = 0.1$. (c) Etch bias is a measure of the amount by which the etched film undercuts the mask at the mask film interface. Fig. (c) Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted by permission.

lateral etching proceeds more rapidly than the process in which $L_R = 0.1$, and thus leads to more severe undercutting. As a result, we see that L_R is one of the variables which impacts feature size, as well as edge profile. We shall also see that other parameters play a role in controlling such characteristics of the feature attributes as size and edge profile.

In fabrication technologies that are performed using isotropic etching processes, the problem of etch bias is handled by specifying an appropriate amount of compensation in the mask dimensions. For example, if the bias of an etch process is 1 μm, a 6 μm feature on the *mask* can be used to produce a desired 5 μm feature on the *wafer*. Unfortunately, for VLSI technologies in which the pattern dimensions approach the thicknesses of the films being patterned, the margin for compensation diminishes, and a higher degree of anisotropy is required. For practical purposes this situation arises when pattern features become smaller than ~3 μm. Under these circumstances, isotropic etching processes become inadequate, and processes that provide higher degrees of anisotropy need to be employed.

Selectivity, Over-Etch, and Feature Size Control

In earlier sections, only the etching characteristics of the film were considered when examining the relationship between bias and edge profile, and degree of etch anisotropy. We assumed that the mask was not attacked by the etchant, and did not consider that the layers under the etched film can also be attacked by the etchant. In fact, both mask material and underlying layer materials are generally etchable, and these effects may play a significant role in specifying etch processes. Note that the underlying material subject to etchant attack may be either the silicon wafer itself, or a film grown or deposited during a previous fabrication step. The ratio of etch rates of different materials is known as the *selectivity of an etched process*[12]. Thus both: 1) the selectivity with respect to the mask material; and 2) the selectivity with respect to the substrate materials are important characteristics of an etch process.

The *selectivity with respect to the mask material*, S_{fm}, plays a role in determining the etched feature sizes. The *selectivity with respect to substrate*, S_{fs}, can impact performance and yield. Film thickness and etch rate non-uniformities increase the required values of S_{fm} and S_{fs} because the etch processes need to be continued beyond the point at which the mean film thickness is completely etched (cleared). Such additional etching is referred to as *overetch*. For example, due to overetch requirements, when contact holes are to be etched in SiO_2 it is desirable that the etch rate decrease when the silicon substrate is reached. In this case, a process with high selectivity with respect to substrate is necessary.

For many wet-etch processes, both S_{fm} and S_{fs} are very high, and thus neither the mask or substrate materials are affected very much during such well-controlled wet-etch procedures. However for dry-etch processes, these desirable circumstances are rarely encountered. Thus, it is necessary to calculate the selectivities that an etching application will require, so that dry-etch processes which are able to meet such specifications can be selected or developed.

Determining the Required Selectivity With Respect to Mask Materials, S_{fm}

The required selectivity with respect to the mask, S_{fm} is dependent on several factors including: a) film thickness uniformity; b) film etch rate uniformity; c) mask etch rate uniformity; d) the edge profile of the mask; e) the anisotropic etch rate of the mask; and f) the maximum acceptable loss of line width of the patterns being etched[11]. These factors can be quantified with the assistance of the information given in Fig. 7.

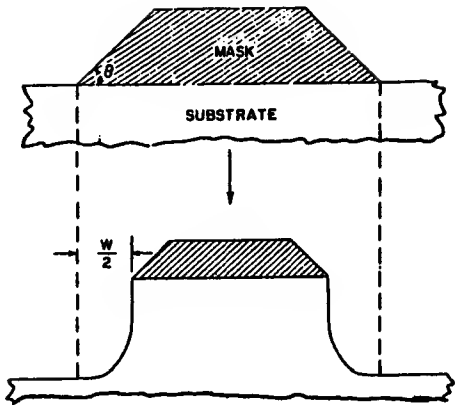

Fig. 7 The evolution of an etched feature when the mask has a finite etch rate. The difference between the intended pattern width and the actual linewidth is W. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted by permission.

For example, assume we wish to etch a film that has some degree of thickness non-uniformity. This film has a mean thickness, h_f, a maximum thickness, $h_f(1 + \delta)$, and a minimum thickness, $h_f(1 - \delta)$, where δ is a dimensionless parameter with a value $0 \leq \delta < 1$. Assume also that the film etch rate is somewhat nonuniform. That is, a mean etch rate, v_f, of the film exists over the wafer area, and that v_f varies between $v_f(1 + \phi_f)$ and $v_f(1 - \phi_f)$, where ϕ_f is again a dimensionless parameter of value $0 \leq \phi_f < 1$. In order to insure that the maximum loss of linewidth is less than or equal to the allowable linewidth loss, this effect must be determined for the worst-case etching condition on the wafer. Maximum linewidth loss occurs where the film is thickest, $[h_f(1 + \delta)]$, and at wafer locations where the film etch rate is slowest, $v_f(1 - \phi_f)$. Thus, the time required to etch the film at such locations is the longest, and is given by:

$$t_c = \frac{h_f(1+\delta)}{v_f(1-\phi_f)} \tag{4}$$

If it is independently determined that a fractional overetch time, Δ, is also required, then the total etch time, t_t, is increased to:

$$t_t = \frac{h_f(1+\delta)(1+\Delta)}{v_f(1-\phi_f)} \tag{5}$$

During the etch time, the mask will be eroded as shown in Fig. 7. If the mask material is removed with maximum vertical and horizontal etch rates, v_v and v_l, respectively, then the edge of the mask will retreat from its original locations by a distance, W /2, given by:

$$\frac{W}{2} = [v_v \cot\theta + v_l]\, t_t \tag{6}$$

where θ is defined in Fig. 7, and the total loss of linewidth is 2(W /2). The loss of linewidth dimension of the mask, W due to erosion during t_t, is then found by substituting Eq. 5 into Eq. 6 to give:

$$W = 2\frac{v_v}{v_f}h_f\frac{(1+\delta)(1+\Delta)}{(1-\phi_f)}\left[\cot\theta + \frac{v_l}{v_v}\right] \quad (7)$$

The mask etch rates are generally also nonuniform, and the nonuniformity is expressed as $v_v = v_m(1 \pm \phi_m)$, where v_m is the mean mask etch rate and ϕ_m is a dimensionless parameter. For the worst case again, we select the condition where the mask etch is fastest. Thus, $v_m(1+\phi_m)$ is substituted into Eq. 7 for v_v. In addition, selectivity with respect to the mask is defined as $S_{fm} = v_f/v_m$. From Eq. 3 the mask lateral etch rate ratio is $v_v/v_L = L_R = 1 - A_m$. Using these definitions and rearranging Eq. 7 we get the required S_{fm} as:

$$S_{fm} = \frac{h_f}{W}U_{fm}[\cot\theta + (1-A_m)] \quad (8)$$

where;

$$U_{fm} = \frac{[(1+\delta)(1+\Delta)(1+\phi_m)]}{(1-\phi_f)} \quad (9)$$

and U_{fm} is the uniformity factor that accounts for the simultaneous occurrence of worst-case conditions that leads to the greatest mask erosion, and thus maximum linewidth loss. Figure 8 shows a set of curves of required S_{fm} which apply to the specific case of $\phi_m = \phi_f = 0.1$, $\delta = 0.05$, and $\Delta = 0.2$. For these conditions $U_{fm} = 1.54$, and the curves are plotted for various h_f/W ratios and various degrees of mask edge angles, θ, and etch anisotropy, A.

Example: Assume that a 1 μm film is to be patterned with a completely anisotropic etch process and thus the only loss of feature linewidth is due to mask erosion. In addition, let the mask and film etch rate uniformities both be 10%, and the film thickness uniformity be 5%. In addition, a 20% overetch is required. Find the required selectivity to the mask for a maximum 0.2 μm linewidth loss if the resist profile angle is, a) 60%, and b) 90% for, 1) isotropic mask etching, and 2) completely anisotropic mask etching.

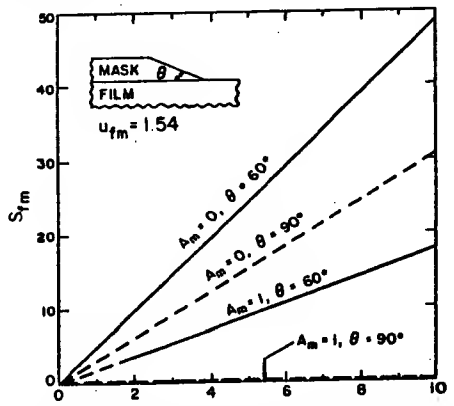

Fig. 8. Selectivity, S_{fm}, needed with respect to the mask, plotted as a function of the ratio of film thickness to loss of linewidth for various mask profiles, and the extremes of isotropic & anisotropic mask etching. Copyright 1983 Bell Telephone Laboratories, Inc, reprinted by permission.

Solution: Figure 8 can be used to solve this problem since the curves were generated for the given worst case nonuniformity values from Eq. 8. Note that for other etch rate and thickness non-uniformities, different curves need to be derived. For this film $h_f = 1.0\ \mu m$, and $W = 0.2\ \mu m$, so $h_f/W = 5$. From the curves of Fig. 7 we see that the following S_{fm} are required:

a) $S_{fm}(\theta = 60°, A = 0) = 23$
b) $S_{fm}(\theta = 60°, A = 1) = 9$
c) $S_{fm}(\theta = 90°, A = 0) = 15$
d) $S_{fm}(\theta = 90°, A = 1) = 0$

It can be seen from this example that anisotropic etch processes, combined with vertical walled etch mask profiles, result in the most precise pattern transfers. However, there is also another phenomenon associated with sputtering and dry-etching, referred to as *faceting* which can also contribute to mask erosion. Faceting is discussed in more detail Chap. 10.

Determining Required Selectivity With Respect to Substrate, S_{fs}

The necessary selectivity with respect to substrate, S_{fs}, is also calculated by considering the worst-case condition[13]. That is we assume the thinnest part of the film to be etched lies over the region of the substrate that experiences the highest etch rate. We use this assumption to calculate a uniformity factor, U_{fs}. We then multiply U_{fs} by the ratio h_f/h_s (where h_f is the mean film thickness, and h_s is the maximum allowable penetration depth of the substrate layer) to arrive at the required S_{fs}, or:

$$S_{fs} = \frac{h_f}{h_s} U_{fs} \qquad (10)$$

and

$$U_{fs} = \left[\frac{\phi_f(2 + \Delta + \Delta\delta) + \delta(2 + \Delta) + \Delta}{(1 - \phi_f^2)} \right] \qquad (11)$$

where ϕ_f, Δ, and δ are defined as in the last section that derived S_{fm}. We see from Eq. 10 that if the film is perfectly uniform ($\delta = \phi_f = 0$) and if no overetching is required ($\Delta = 0$), selectivity with respect to the substrate would not be an issue of concern since U_{fs} would equal zero. However, since these conditions are not representative of actual conditions, Eq. 10 is useful in determining realistic S_{fs} values.

There is another factor, even more important than film and etch rate non-uniformities, which dictates the degree of overetching when anisotropic etch processes are employed. That is, as shown in Fig. 9a, when material is cleared from a planar region on a wafer, residual material at steps has still not been removed. Thus, additional etching beyond the point at which the planar regions have cleared must be used to remove such residual material (sometimes referred to as *stringers* or *picket fences*). As shown in Fig. 9b, failure to remove this material can lead to unwanted electrical shorting paths between adjacent lines. From Fig. 9a and b, it can be seen that for completely anisotropic etch processes (A = 1), the fractional overetch, Δ, required to clear such residual material, is h_1/h_2.

Example: Given a 2500 Å polysilicon layer that passes over both 5000 Å field-oxide regions and 250 Å gate oxide layers. Assume that a completely anisotropic

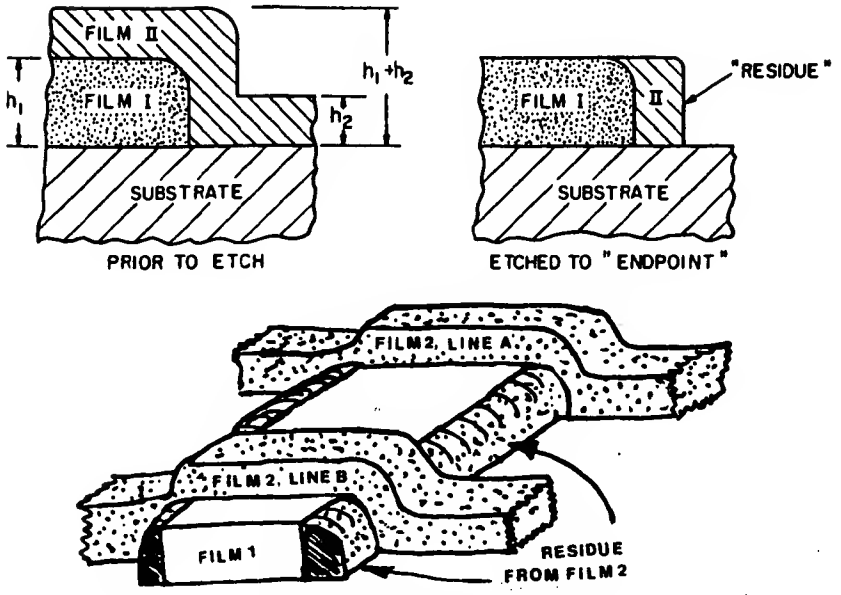

Fig. 9 If etching is anisotropic, overetching is needed to remove residual materials at steps. The degree of anisotropy, A = 1 in the example shown. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted by permission.

etch process will be used to etch the polysilicon, and that the polysilicon film thickness uniformity is 5%, and the uniformity of etching is 10%. Find the required S_{fs} for this process, if the etching is to be stopped immediately after the polysilicon is completely etched.

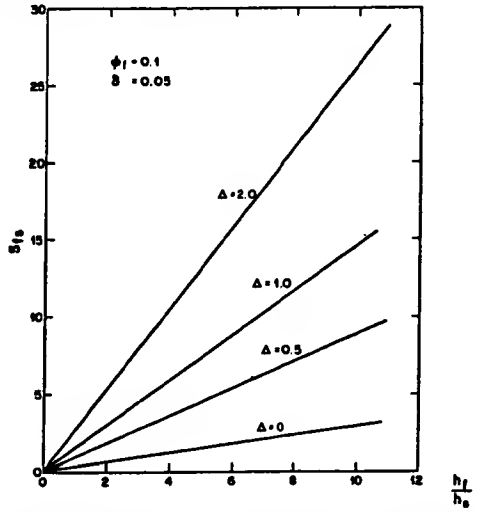

Fig. 10 The selectivity needed with respect to substrate, S_{fs}, is plotted as a function of the ratio of film thickness to the amount of substrate removed for various amounts of overetching. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted by permission.

Solution: Since the polysilicon must pass over 5000 Å steps (e.g.where field and gate oxide meet), the thickness of the poly at the step will be (from Fig. 8):

$$h_1 + h_2 = 5000\ Å + 2500\ Å = 7500\ Å.$$

This is the thickness of polysilicon that must be removed by an anisotropic etch procedure. Thus, $\Delta = h_1/h_2 = 2$. The maximum allowable penetration of the fractional overetch required to completely remove the residual material at the steps underlying gate oxide layer is $h_s = 250$ Å. Any more penetration will remove all of this oxide and expose the silicon substrate material to the etchant. Thus, $h_f/h_s = 2500/250 = 10$. From Fig. 10, which can be applied to this problem, we find that:

$$S_{fs} = 25.$$

Note the curves of Fig. 8 and Fig. 10 were derived for specific mask, film, and etch rate nonuniformities. Each etching process, however has its own set of characteristics and appropriate curves for a specific process need to be derived using Eq. 8 and Eq. 10 with those values.

Combined Impact of the Requirements of Anisotropy and Selectivity

A high degree of anisotropy is a desirable feature of an etch process for fine feature patterning since in such applications very little etch bias can be permitted. A highly selective etch rate with respect to the mask is needed to maintain feature size control. An adequate degree of selectivity with respect to underlying materials is also necessary in order to prevent removal of previously processed portions of the circuit. However, when anisotropic etching is performed in the presence of stepped topography, we have shown that the remaining residual material at the steps requires additional overetching beyond even that required by etch rate and "normal" film thickness nonuniformities. Thus, the mandate that calls for anisotropic etch processes ends up also driving the selectivity requirements even higher.

Loading Effects

When the etch rate is dependent upon the amount of etchable surface exposed to the etchant, the phenomenon is called a *loading effect*. The effect arises when there are a limited number of etchant species available to etch a material. When these are depleted, etching cannot continue until new etching species arrive at the surface. Loading effects are most commonly encountered in dry-etch processes where they can occur in a variety of different conditions. These include: a)

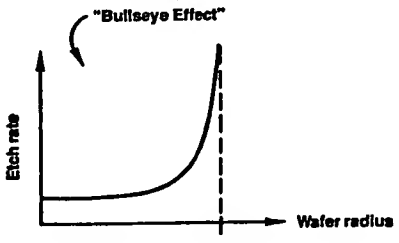

Fig. 11 Example of "bullseye" etch nonuniformirty.

etch rate is dependent upon the number of wafers present in the chamber. In such cases, as the number of wafers in the system is increased, the rate of consumption of etchant species also increases. This may result in a loading effect that will lead to a slower overall etch rate; b) the etch rate depends on the amount of area on the wafers, or on a single-wafer in single-wafer etching systems, that has etchable material exposed. Note that this exposed etchable area can even change during an etch process. That is, upon the clearing of an etching film from the planar regions of a surface, much less residual material remains. Thus, more etchant species may be available to attack any residues, but also the exposed sidewalls of the etchable film. As a result, lateral etch rate changes during overetch time may be a side effect of local loading effects.

Gas flow effects may also combine with loading effects to cause etch rate nonuniformities. That is, the location of a wafer in a chamber, as well as the number present in the chamber, may impact the etch rate. The *bullseye effect* sometimes observed in dry etching, in which the film at edges of a wafer is etched more quickly than at the center (Fig. 11), is due to depletion of etchant species at the wafer center. More etchant species can arrive at the wafer near its edge than from just above the wafer surface. Techniques to minimize loading effects are described in Chap. 16.

WET ETCHING TECHNOLOGY

Wet etching processes are generally isotropic. As such we have pointed out that they are inadequate for defining features less than about 3 μm wide. Nevertheless for those process that involve patterning of linewidths greater than 3 μm, wet etching continues to be a viable technology. Since it turns out that a significant fraction of semiconductor products are still being fabricated with such large geometries, wet etching should not be ignored. In this section we present some of the more important aspects of wet etching technology for current processing needs. In addition more detailed information can be found in references listed at the end of the chapter[1,14,17,18,10].

The reason wet etching has found widespread acceptance in microelectronic fabrication is that it is a low cost, reliable, high throughput process with excellent selectivity for most wet etch processes, with respect to both mask and substrate materials. Some recent refinements to wet-etching equipment have in fact increased these advantages, including: a) the automation of wet stations; b) the placing of wet etch process steps under microprocessor control, to improve reproducibility of etching conditions from run-to-run, and to give the process engineers better control of the equipment functions by preventing unauthorized process changes; c) point-of-use filtration of etchants to prolong their use by removing etch process generated defects; and d) the development of spray etching. Such advances make it likely that wet etching will continue to find extensive use in semiconductor fabrication for the foreseeable future[15,16].

On the other hand, besides the 3 μm limitation, wet etching is subject to the following disadvantages: a) higher cost of etchants and DI water compared to dry etch gas expenses; b) increased personnel safety hazards from chemical handling; c) exhaust fumes and the potential of explosions; d) resist adhesion problems; and e) bubble formation and incomplete wetting of wafer surfaces by the chemical etchants leading to incomplete etching and etching non-uniformities.

In general a wet etch process can be broken down into three steps: 1) diffusion of the reactant to the reacting surface; 2) reaction; and 3) diffusion of the reaction products from the surface[20]. The second step can obviously be further differentiated into adsorption prior to, and desorption subsequent to, the actual reaction step. The slowest of the steps will be *rate-controlling*. That is, the rate of that step will be the rate of the overall reaction.

Chemical etching can occur by several processes. The simplest involves dissolution of the